on an electroplated layer on a substrate of a difficult to solder material. Dale does not disclose either of these arrangements.

Dale discloses a method of securing a semiconductor body to a substrate by pressure bonding. As described in column 3, line 13 of Dale, a malleable metal layer of soft solder is disposed between a semiconductor body and a substrate, and a pressure of 1 - 5 tons per square inch is applied at a temperature of 75 - 300°C. Dale states that coatings of various materials can be formed on the substrate or the semiconductor body opposing the solder layer, but there is no disclosure or suggestion of any of the coatings being formed by electroplating. The only specific method of forming a coating which Dale describes is silk screening for the case in which a coating is formed on a ceramic (column 5, line 33). The word electroplating never even appears in Dale. The Official Action states that column 5, lines 16 - 54 disclose an electroplated layer on a substrate, but the Applicant cannot find any mention of electroplating in the cited passage or anywhere else in Dale. In all the examples of Dale, the solder is in the form of a foil, but Dale mentions briefly in column 6, lines 46 - 51 that the solder can be applied as a coating by dip soldering. However, there is no mention of the dip coating being formed anywhere except directly on the substrate or semiconductor body, and there is no disclosure or suggestion of performing dip coating on an electroplated layer.

Therefore, as Dale does not disclose a hot dip solder plating layer formed on an electroplated layer, it does not disclose all the features of independent claims 16 or 20 and so

cannot anticipate these claims or claims 17 - 19 and 21 - 24 which depend therefrom. These claims are therefore allowable.

Amended claim 24 further patentably distinguishes the present invention from Dale. Amended claim 24 states that the portion to be soldered of claim 20 (which has a hot dip solder plating layer formed on an electroplated layer) is a lid of a packaged electronic part. Amended claim 24 is the same as original claim 24 except that the other choices of portions to be soldered (a lead frame for an electronic part, a battery terminal, a shield of a module, or a connector for a surface mounted part) in original claim 24 have been made into separate dependent claims to improve the readability of the claims. The Official Action states that Dale teaches use of a soldered portion to join a lid of a packaged part, but this does not appear to be the case. Column 9, lines 64 - 67 of Dale mention in passing that one example of a device to which the method of Dale is applied has a glass wall 63 with a sealing ring 67 of Kovar for use in attachment of a case lid, but there is no mention of the structure of the lid or of how the lid is joined to the wall 63. The lid is in fact irrelevant to the method of Dale, which is concerned solely with how to join a <u>semiconductor body</u> to a substrate. Thus, Dale clearly does not anticipate claim 24.

Original claim 24 also states that the portion to be soldered of claim 20 could be a shield of a module. This feature of original claim 24 is now in dependent claim 33. The Official Action, referring to column 10, lines 46 - 56 of Dale, states

that the soldered portion in Dale may be used to join module devices. If the Official Action is implying that Dale anticipates the feature of original claim 24 now in claim 33, then the Official Action is incorrect. Column 10, lines 46 - 56 of Dale state that the embodiment of Figure 7 is used in the manufacture of a transmitting transistor module device, but the similarity between this description and claim 33 ends with the word "module". Dale contains no reference to any shield of a module, so it cannot anticipate original claim 24 or new claim 33.

Claims 16 - 25 and 27 - 29 were rejected under 35 USC 102(b) as anticipated by Fister et al (U.S. Patent No. 4,978,052, referred to below as Fister). This rejection is respectfully traversed.

Independent claim 16 describes a solder coated material including a hot dip solder plating layer on an electroplated layer. Independent claim 20 describes a portion to be soldered including a hot dip solder plating layer on an electroplated layer. Independent claim 25 describes a method including passing a difficult to solder material having an electroplated layer through a molten solder bath. Fister does not disclose such arrangements or such a method.

Fister discloses a system for attaching a semiconductor die to a substrate. In order to reduce thermal strains due to the mismatch between the coefficient of thermal expansion of a high conductivity substrate and a semiconductor die, a metallic buffer

is disposed between the substrate and the die and is preferably sealed to the substrate by a layer of solder. The manufacture of the system of Fister nowhere involves forming a hot dip solder plating layer on an electroplated layer.

Figure 1 of Fister discloses an embodiment in which a solder preform 18 (see column 7, line 32) is disposed on a substrate 14 beneath a semiconductor die 12 and a buffer 16. There is no hot dip solder plating layer in this embodiment.

Figure 2 of Fister discloses an embodiment in which a layer of solder 18' is disposed between a buffer layer 16' having barrier layers 24 and 26 and oxidation resistant layers 20 and 22 on its top and bottom surfaces and a substrate 14' having a barrier layer 32 and an oxidation resistant layer 36 on its top surface. It is not described how the solder layer 18' is formed, but since it is illustrated as being an independent layer in the exploded view of Figure 2 (as opposed to the way in which plated solder layers 18" are illustrated in the exploded view of Figure 4), the solder layer 18' is clearly a preform, like the preform solder layer 18 of Figure 1. Thus, this embodiment lacks a hot dip solder plating layer on an electroplated layer.

Figure 4 of Fister illustrates an embodiment in which a solder layer 18" is hot dipped directly on both surfaces 28" and 30" of a buffer 16". There is no electroplated layer on which the solder layer 18" is formed, so this embodiment is also lacking a hot dip solder plating layer on an electroplated layer.

Figure 5 of Fister illustrates another embodiment in which a die 12''' is bonded to a substrate 14''' by a solder layer 18'''.

There is no description of the structure of the solder layer 18''', but in light of the similarity between Figure 1 and Figure 5, the solder layer 18''' is clearly a preform, like solder layer 18 of Figure 1. Thus, this embodiment, too, does not have a hot dip solder plating layer on an electroplated layer.

Thus, contrary to the statements in the Official Action, nowhere in Fister is there any disclosure of forming a hot dip solder plating layer atop an electroplated layer, so Fister does not disclose all the features of claims 16, 20, or 25 and cannot anticipate these claims or claims 17 - 19, 20 - 24, and 27 - 29 which depend therefrom. These claims are thus allowable.

Claim 24 further patentably distinguishes the present invention from Fister. Claim 24 states that the portion to be soldered of claim 20 is a lid of a packaged electronic part. The Official Action, referring to column 1, lines 49 - 58 of Fister, states that the method of Fister may be used to join a lid of a packaged part. This statement in the Official Action is incorrect. Fister pertains solely to joining a semiconductor die to a substrate, and column 1, lines 49 - 58 is but background information, explaining that a sealed package in which a semiconductor is housed typically includes a lid. The method which Fister uses to join a semiconductor die to a substrate has nothing to do with how a lid is joined to a base of a semiconductor package. Column 8, lines 15 - 19 of Fister describe how a cap or lid 54 can be mounted on a leadframe 46, and this is by means of a glass seal produced by melting glass 50. Thus, Fister nowhere teaches a soldered lid as claimed in

claim 24 and thus cannot anticipate this claim.

Claims 25, 26, and 28 - 30 were rejected under 35 USC 102(b) as anticipated by Elliott (U.S. Patent No. 5,232,562). This rejection is respectfully traversed.

Claim 25 describes a method of manufacturing a solder coated material including electroplating a difficult to solder material to form an electroplated layer. Elliott does not disclose such a method.

Elliott discloses an electrochemical reduction treatment which performs cleaning of metallic surfaces in preparation for soldering. A reduction treatment liquid is applied to a surface of a component, and then the component is passed through a solder wave in a soldering treatment. The reduction treatment liquid is a liquid which reduces a surface oxide layer to clean a metal surface of oxides. An example of a reduction treatment liquid given in column 2, line 3 of Elliott is a sodium borate solution. Electrochemical reduction is thus totally different in nature from electroplating; it does not form an electroplated layer but instead removes material from a surface on which it is performed. This is why, as pointed out in column 2, line 19 of Elliott, electrochemical reduction is sometimes known as reverse plating.

Thus, as Elliott does not include forming an electroplated layer, it does not include all the steps of claim 25 and so cannot anticipate this claim or claims 26 and 28 - 30 which depend from it. These claims are therefore allowable.

Claims 25 - 28 were rejected under 35 USC 102(b) as anticipated by what the Official Action refers to as "Kato (USPN 5232562)". It is believed that the identification of the reference contains a typographical error and that the Examiner intended to base the rejection on Kato et al (U.S. Patent No. 5,322,205, referred to below as Kato), since "5232562" is the patent number of the Elliott reference, referred to above. This rejection is respectfully traversed.

Amended claim 25 describes a method of manufacturing a solder coating material including forming a hot dip solder plating layer having a thickness of 10 - 50 μm on an electroplated layer. In addition to being amended to include the thickness of the hot dip solder plating layer, claim 25 has been amended to clarify that the molten solder bath forms a hot dip solder plating layer on the electroplated layer. Amended claim 25 is supported by page 9 of the specification as filed. Kato does not disclose or suggest such a method.

Kato discloses a method of joining an aluminum member to a dissimilar member in which a plating layer is formed by electrolysis on the dissimilar material and then the plating layer is dipped in a molten solder to form a solder layer atop the plating layer. However, there is no disclosure in Kato of the thickness of the solder layer and specifically no teaching or suggestion of forming a hot dip solder plating layer having a thickness of 10 - 50 micrometers. As described on page 9, line 21 - page 10, line 2 of the present application, a thickness for a hot dip solder plating layer of 10 - 50 micrometers atop an

electroplated layer is advantageous because if the thickness is less than 10 micrometers, the amount of solder at the time of soldering is inadequate, and soldering defects occur. If the thickness of the hot dip solder plating layer is greater than 50 micrometers, the overall thickness end up being non-uniform, and dripping of solder at the time of soldering, short circuits with neighboring portions, and an increase in the volume of small sealed parts occur. These advantages of the thickness range recited in claim 25 are nowhere suggested, so a person skilled in the art would not arrive at the claimed range based on Kato.

Therefore, since Kato does not teach all the features of amended claim 25, it cannot anticipate this claim or claims 26 - 28 which depend from it. These claims are therefore allowable.

New claims 31 - 42 describe additional features of the present invention. Claims 31 - 40 are allowable as depending from claims 16 or 25. New claim 41 describes a method of forming a packaged electronic part including performing reflow soldering of a lid having an electroplated layer formed on a substrate of the lid and a hot dip solder plating layer formed on the electroplated layer to join the lid to a package. None of the cited references discloses or suggests such a method. As discussed above, the methods of Dale and Fister have nothing to do with joining a lid to a package. Specifically, Dale and Fister pertain to joining a semiconductor body or a semiconductor die to a substrate. Elliott relates to cleaning of metallic surfaces of a circuit board prior to soldering and is unrelated to joining a lid to a package. Kato discloses a method of

joining an aluminum member to a dissimilar member. Kato does not disclose what the two members to be joined are, but from the description of the prior art in column 1, lines 17 - 27 of Kato, it appears that Kato is concerned primarily with overcoming the difficulty in the prior art of joining pipes to each other, and there is no mention or suggestion of joining a lid to a package, as in claim 41. Claim 41 is therefore allowable. Claim 42 is allowable as depending from claim 41.

In light of the foregoing remarks, it is believed that the present application is in condition for allowance, and favorable consideration is respectfully requested.

Respectfully submitted,

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ATTACHMENT A

Marked-up version of the amended claims:

24. (Amended) A portion to be soldered of an electronic part as claimed in claim 20 wherein the portion to be soldered is [a lead frame for an electronic part,] a lid of a packaged electronic part[, a battery terminal, a shield of a module, or a connector for a surface mounted part].

25. (Amended) A manufacturing method for a solder coated material comprising electroplating a difficult to solder material with a material having excellent solderability to form an electroplated layer, and then passing the difficult to solder material through a molten solder bath [and adhering molten solder] to <u>form a hot dip solder plating layer having a thickness of 10 - 50 micrometers on</u> the electroplated layer.